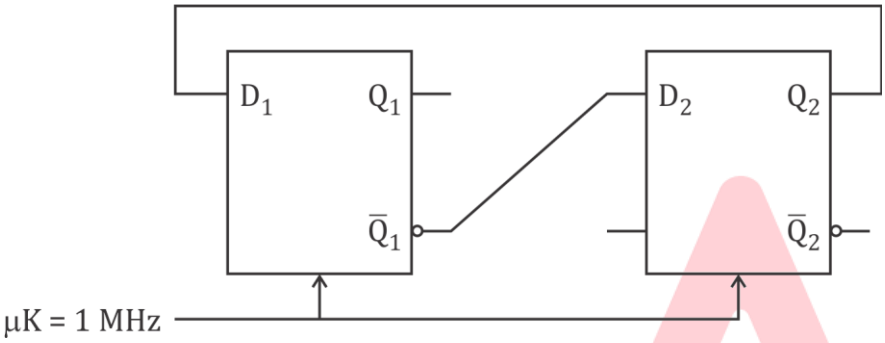
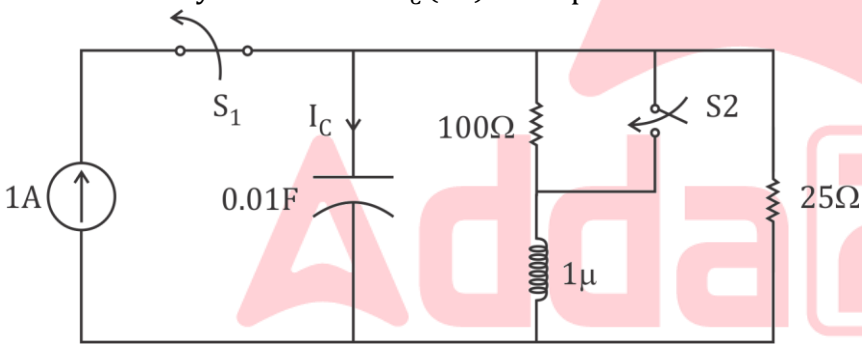
GATE 2023 Electronics Engineering

Q1. In a given sequential circuit initial state are $Q_1 = 1$ and $Q_2 = 0$. For a clk frequency of 1 MHz, the frequency of signal Q_2 in KHz is _____.



Q2. The switch S_1 was closed and S_2 was open for a long time. At t =0 switch S_1 is opened and S_2 is close simultaneously. The value of $I_C(0^+)$ in amp is

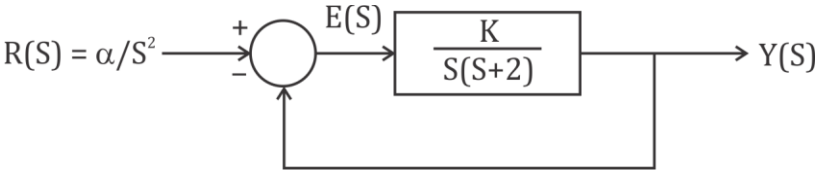


(a) –1
(b) 0.2
(c) 1
(d) 0.8

Q3. The state equation of 2nd order system is $\dot{x}(t) = Ax(t), x(0)$ is the initial condition suppose λ_1 and λ_2 are two distinct eigen values of A and V_1 and V_2 are the corresponding eigen vectors. For constant α_1 and α_2, the solution $x(t)$ of the state equation is

(a) $\Sigma_{i=1}^{2} \alpha_i e^{4\lambda_i t} V_i$
(b) $\Sigma_{i=1}^{2} \alpha_i e^{2\lambda_i t} V_i$
(c) $\Sigma_{i=1}^{2} \alpha_i e^{\lambda_i t} V_i$
(d) $\Sigma_{i=1}^{2} \alpha_i e^{3\lambda_i t} V_i$

Q4. A closed loop system is shown in the figure where k > 0 and $\alpha > 0$. The steady state error due to ramp input $(R(s) > \alpha/S^2)$ is given by



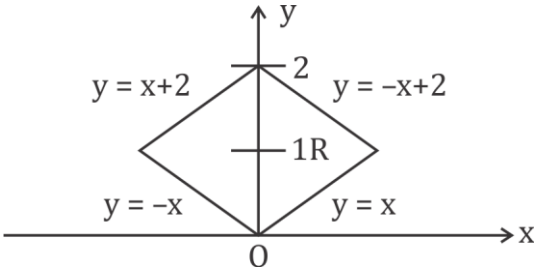
(a) $\frac{\alpha}{4k}$

(b) $\frac{2\alpha}{k}$

(c) $\frac{\alpha}{2k}$

(d) $\frac{\alpha}{k}$

Q5. The value of the integral $\iint xy\,dx\,dy$ over the region R, given in the figure, is ____.



Q6. Let x be $n \times 1$ real column vector with length $L = \sqrt{x^T x}$. The trace of matrix $P = xx^T$ is

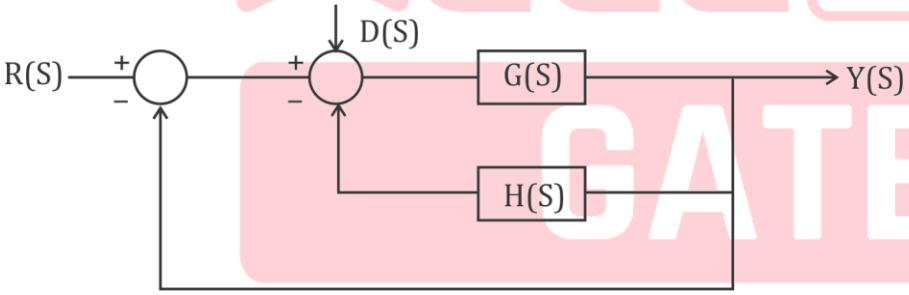
(a) $L^2/2$

(b) L^2

(c) $L^2/4$

(d) L

Q7. In the full block diagram $R(s)$and $D(S)$ are 2 inputs. The opposite $Y(S)$ is expressed as $T(S) = G_1(S)\,R(S) + G_2(S)\,D(S)$, $G_1(S)$ and $G_s(S)$ are given by



(a) $G_1(S) = \frac{G(S)}{1+G(S)+G(S)H(S)}$ and $G_2(S) = \frac{G(S)}{1+G(S)+G(S)H(S)}$

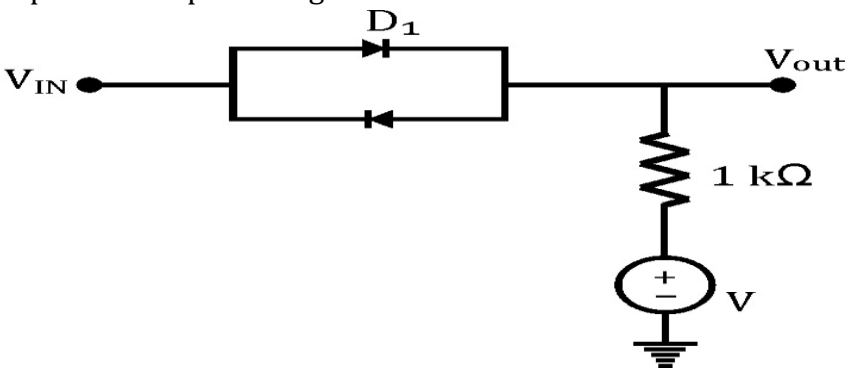
(b) $G_1 = \frac{G}{1+G+GH}$ $G_2 = \frac{G}{1+G+H}$

(c) $G_1 = \frac{G}{1+G+H}$ $G_2 = \frac{G}{1+G+H}$

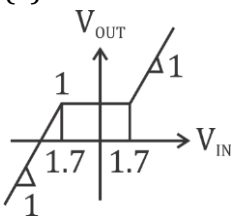
(d) $G_1 = \frac{G}{H+G+H}$ $G_2 = \frac{G}{1+G+GH}$

Q8. A sample and hold circuit is complemented using a resistive RAT switch and a capacitor with time constant of 1 μs. The time 2 m for the sampling switch to stay closed to charge a capacitor adequately to a full scale voltage of 1 V with 12-bit accuracy is _____ μs.

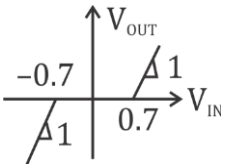
Q9. In the circuit shown below D_1 and D_2 are silicon circle with cut in voltage of 0.7V V_{IN} and V_{OUT} are input and output voltage in volt. The T.C. is



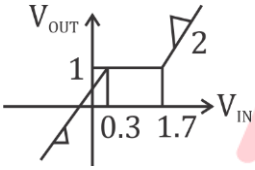
(a)



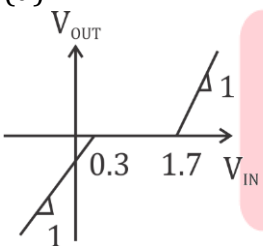
(b)



(c)



(d)



Q10. The value of line integral $\int_P^Q (Z^2 dx + 3y^2 dy + 2xz\, dz)$ along the straight line joined the points $P(1, 1, 2)$ and $Q(2, 3, 1)$ is

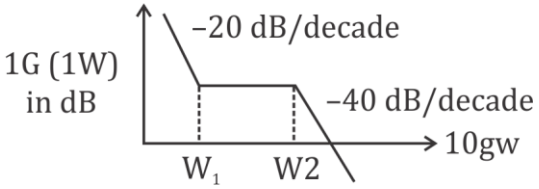
(a) 20

(b) –5

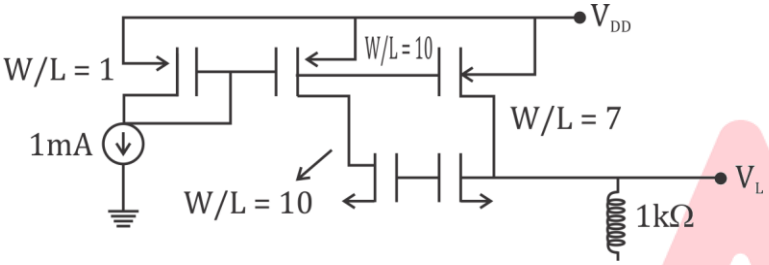
(c) 29

(d) 24

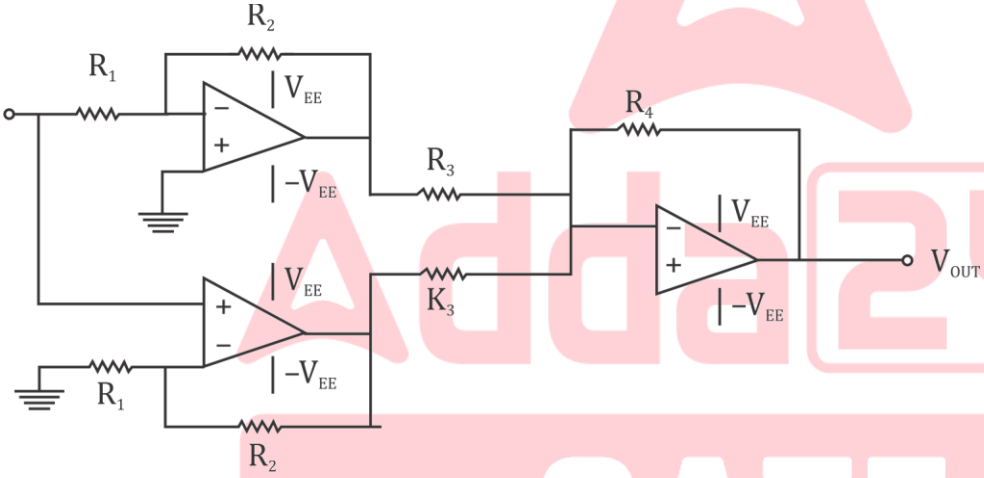
Q11. The asymptotic magnitude Bode phot of a minimum phase system is shown in the figure. The T.F of the system is $G(S) = \frac{K(S+Z)^a}{S^b(S+P)^c}$ where K, Z, p, a, b and c are positive constants. The value of $(a+b+c)$ is _____.



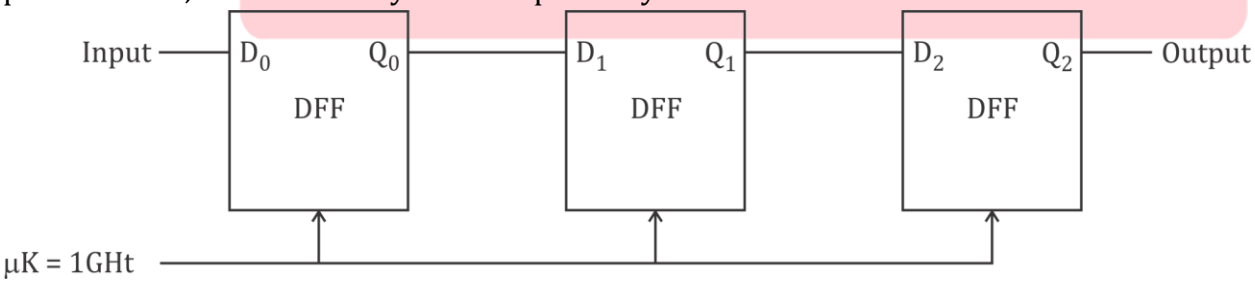
Q12. In the circuit below, the voltage V_C is _____ V.



Q13. The $\frac{V_{OUT}}{V_{IN}}$ of the circuit shown below is

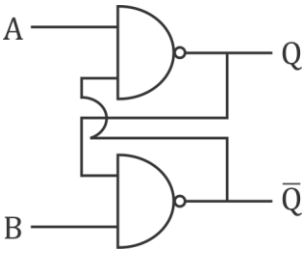


Q14. The synchronous sequential circuit shown below works at a circuit frequency of 1 GHz. The through put in M bitts, and the latency in nS respectively are

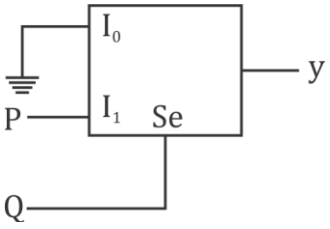


(a) 333.333, 1
(b) 333.33, 3
(c) 2000, 3
(d) 1000, 3

Q15. For the circuit shown below, the propagation delay of each NAND Gate is 1 ns. The critical path delay, in ns is –

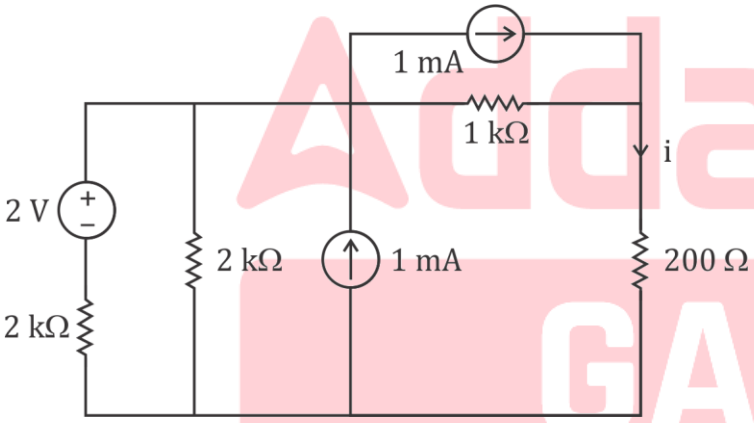


Q16. In the circuit shown below, P and Q are the inputs. The logical function realized by the circuit shown below is

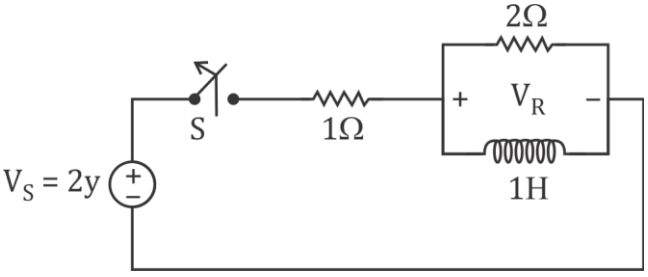


(a) $Y = P + Q$
(b) $Y = \overline{P + Q}$
(c) $Y = \overline{PQ}$
(d) $Y = PQ$

Q17. In the circuit shown below, the current i flowing through 200 Ω resistor is _____.



Q18. In the circuit shown below, switch S was closed for a long time. If switch is opened at $t = 0$ the maximum magnitude of the voltage V_R in volt is _____.



Q19. The voltage of contour integral $\oint_c \left(\frac{Z+z}{Z^2+2Z+z}\right) dt$, where the contour C is $\left\{Z: \left|Z+1-\frac{3}{2}i\right| = 1\right\}$, taken in the counter clockwise direction is

(a) $\pi(1-j)$

(b) $-\pi(1-j)$

(c) $-\pi(1+j)$

(d) $\pi(1+j)$

Q20. The open loop T.F of a unity negative f/b system is $G(S) = \frac{K}{S(1+ST_1)(1+ST_2)}$ where, K, T_1, T_2 are positive constants. The phase cross over frequency in rad/sec.

(a) $\frac{1}{T_2\sqrt{T_1}}$

(b) $\frac{1}{\sqrt{T_1T_2}}$

(c) $\frac{1}{T_1\sqrt{T_2}}$

(d) $\frac{1}{T_1T_2}$

Q21. Let $V_1 = \begin{bmatrix}1\\2\\0\end{bmatrix}$ and $V_2 = \begin{bmatrix}2\\1\\3\end{bmatrix}$ be two vectors. The value of coefficient α is the expression $V_1 = \alpha V_2 + e$. Which minimizes the length of error vector is,

(a) $-\frac{2}{7}$

(b) $\frac{7}{2}$

(c) $-\frac{7}{2}$

(d) $\frac{2}{7}$

Q22. A series RLC circuit has a Quality factor Q of 1000 at a centre frequency of 10^6 rad/sec. The possible value of RLC are

(a) $R = 0.001\ \Omega, L = 1\mu H$ and $C = 1\ \mu F$

(b) $R = 1\Omega, L = 1\mu H$ and $C = 1\mu H$

(c) $R = 0.01\ \Omega = L = 1\ \mu H\ and\ C = 1\mu F$

(d) $R = 0.1\ \Omega, L = 1\ \mu H$ and $C = 1\ \mu F$

Q23. Let the given vector of the matrix B be $\{\lambda_K |\ 1 \le K \le n\}$ and $\{V_K |\ 1 \le K \le n\}$, respectively. For any invertible matrix P, the sets of eigen value and eigen vector of matrix A, where $B = P^{-1}AP$, respectively are

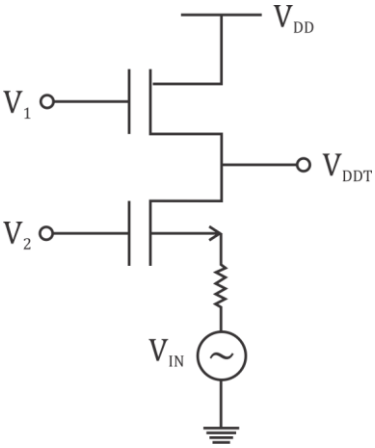
(a) $\{\lambda_K |\ 1 \le K \le n\}$ and $\{V_K |\ 1 \le K \le n\}$

(b) $\{\lambda_K \det(A) |\ 1 \le K \le n\}$ and $\{Pv_K | 1 \le K \le n\}$

(c) $\{\lambda_K |\ 1 \le K \le n\}$ and $\{PV_K |\ 1 \le K \le n\}$

(d) $\{\lambda_K |\ 1 \le K \le n\}$ and $\{P^+V_K \le 1 \le K \le n\}$

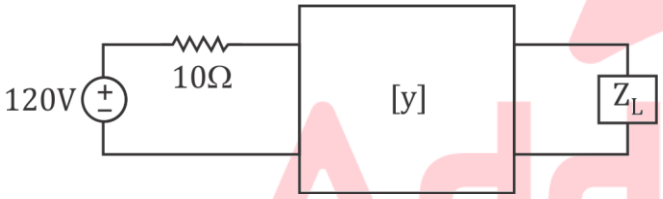
Q24. In the circuit shown below V_1 and V_2 are bias voltage. Based on input and output impedance the circuit behave as



(a) Voltage control source
(b) VCCS
(c) CCCS
(d) CCVS

Q25. For the 2-port network shown below, the $[Y]-$ parameter is given as $[Y]=\frac{1}{100}\begin{bmatrix}2 & -1\\ -1 & 4/3\end{bmatrix}S$

The value of load impedance in Ω, for maximum power transfer will be _____.



Q26. A cascade of common source amplifier in a unity gain feedback configuration oscillate when
(a) Closed 100 p gain is greater than 1 and phase shift is less than 180°
(b) Close 100 p gain is less then 1 and phase shift is greater than 180°
(c) Close 100 p gain is less then 1 and phase shift is less than 180°
(d) Close 100 p gain is greater then 1 and phase shift is greater than 180°