

WELCOME TO **Adda247**

*"If you can think, you can
Achieve"
So start thinking..*

*Renu Raj Garg
M.Tech (VLSI Design)
13 Year of Teaching
Experience
Worked 10 Year in NTRO*

GATE 2024



प्रचण्ड Batch

COMMUNICATION

TIME- 9:00PM

YT

RENU SIR



Chapter-2

Digital Communications

In today's lecture we will cover the following Topics :

1. *Basics of Digital Communication*
2. *Sampling Theorem* ✓✓

Use Code Y505 | Communications for GATE 2024

Adda247

BILINGUAL

PRACHAND BATCH FREE FOR ALL

ELECTRICAL,
ELECTRONICS COMMUNICATION ENGINEERING

GATE 2024 & ALL PSU's



Start Apr 11, 2023

7:30 AM to 11:30 PM

8PM → 3
11AM → 2

You **Tube** Classes Schedule



EE & EC ENGINEERING

EXAM TARGET	SUBJECT	TIME	FACULTY
<u>ALL PSUs</u>	<u>ENGINEERING MATHS</u>	<u>11:00 AM</u>	<u>ANANT SIR</u>
<u>GATE 2024-25</u>	<u>NETWORK THEORY</u>	<u>6:00 PM</u>	RAVI SIR
GATE 2024-25	<u>ELECTRICAL MACHINE</u>	<u>7:30 PM</u>	SANTAN SIR
GATE 2024-25	<u>COMMUNICATION</u>	<u>9:00 PM</u>	RENU SIR

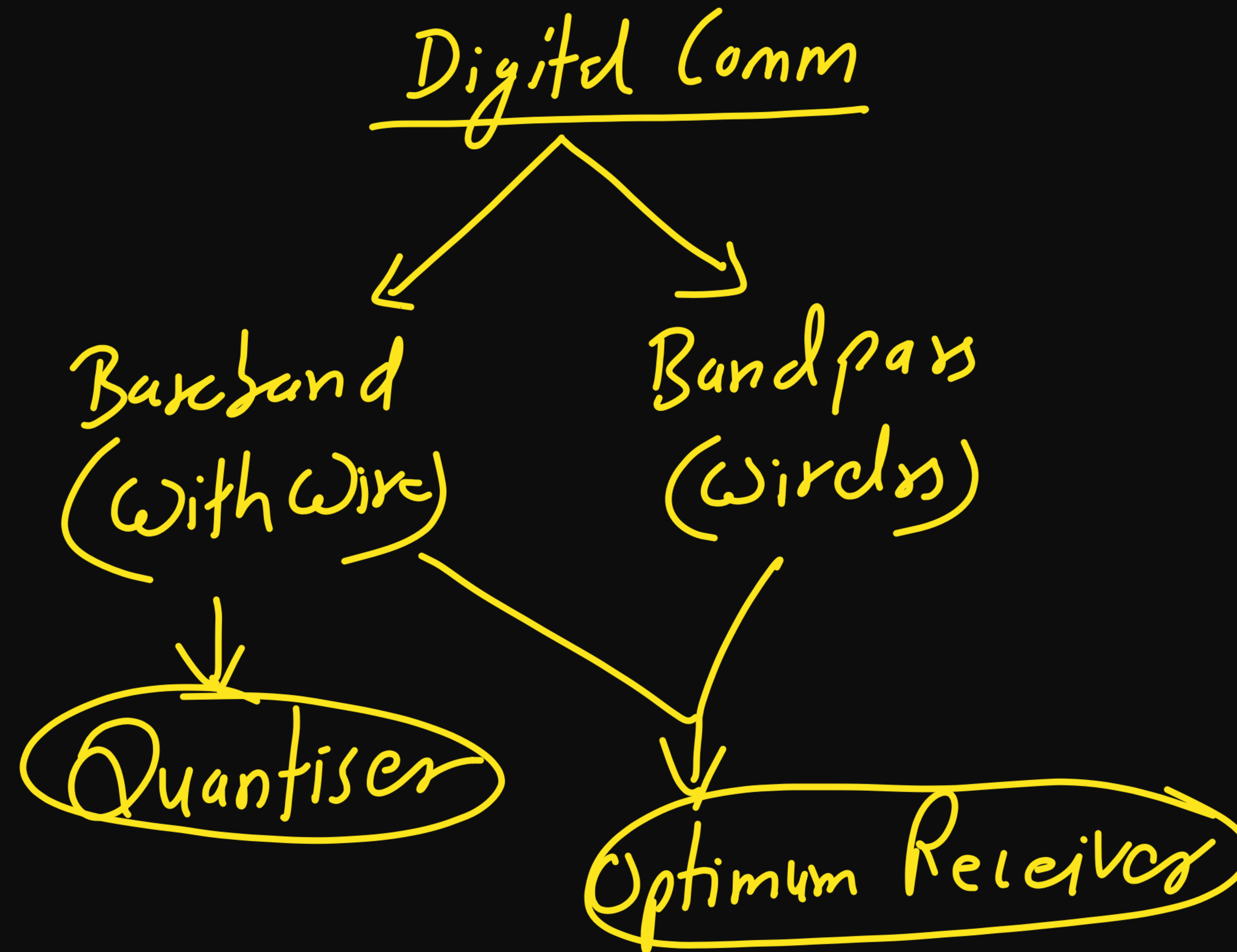
FREE APP CLASS SCHEDULE

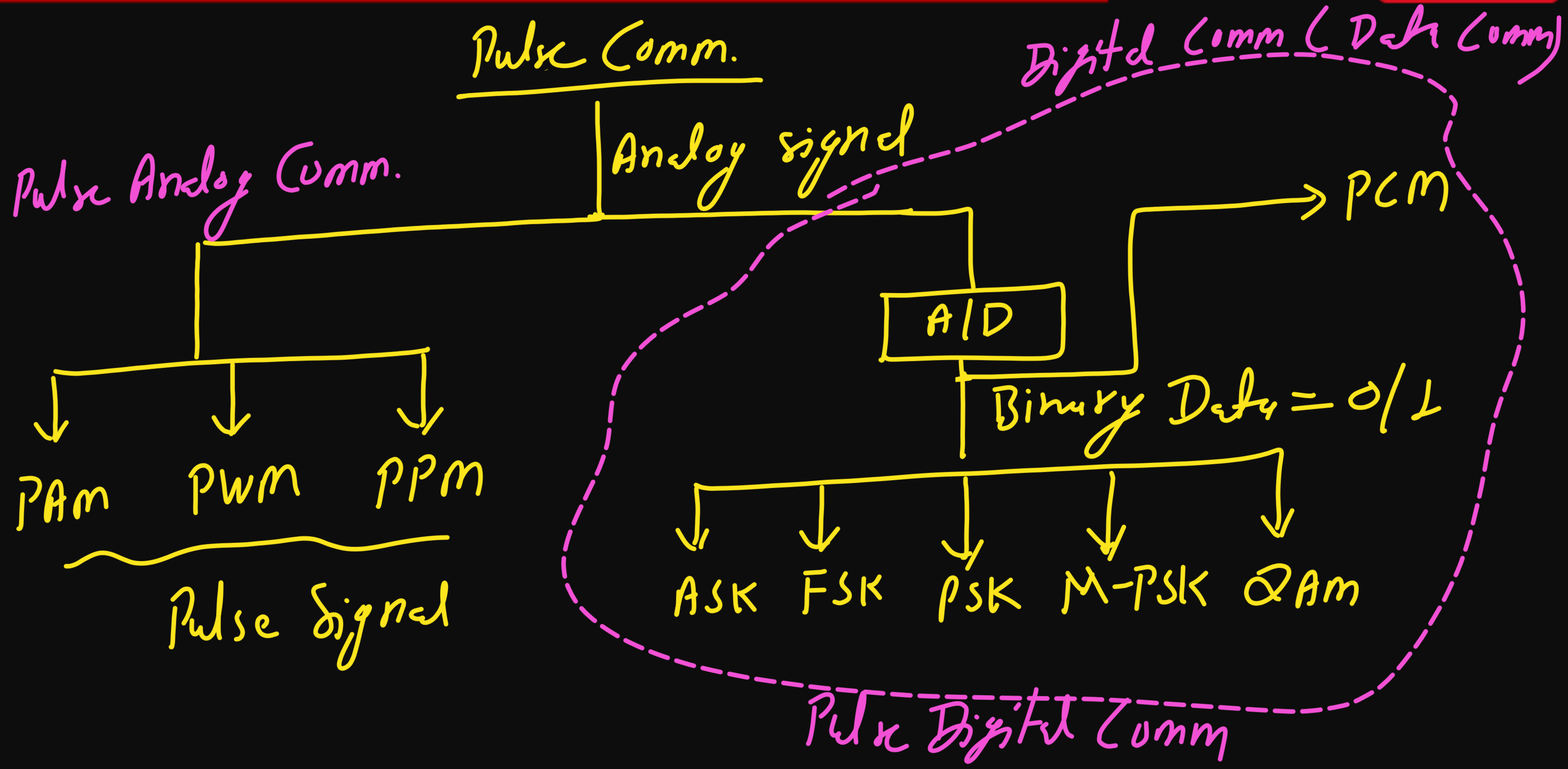


EE & ECE ENGINEERING

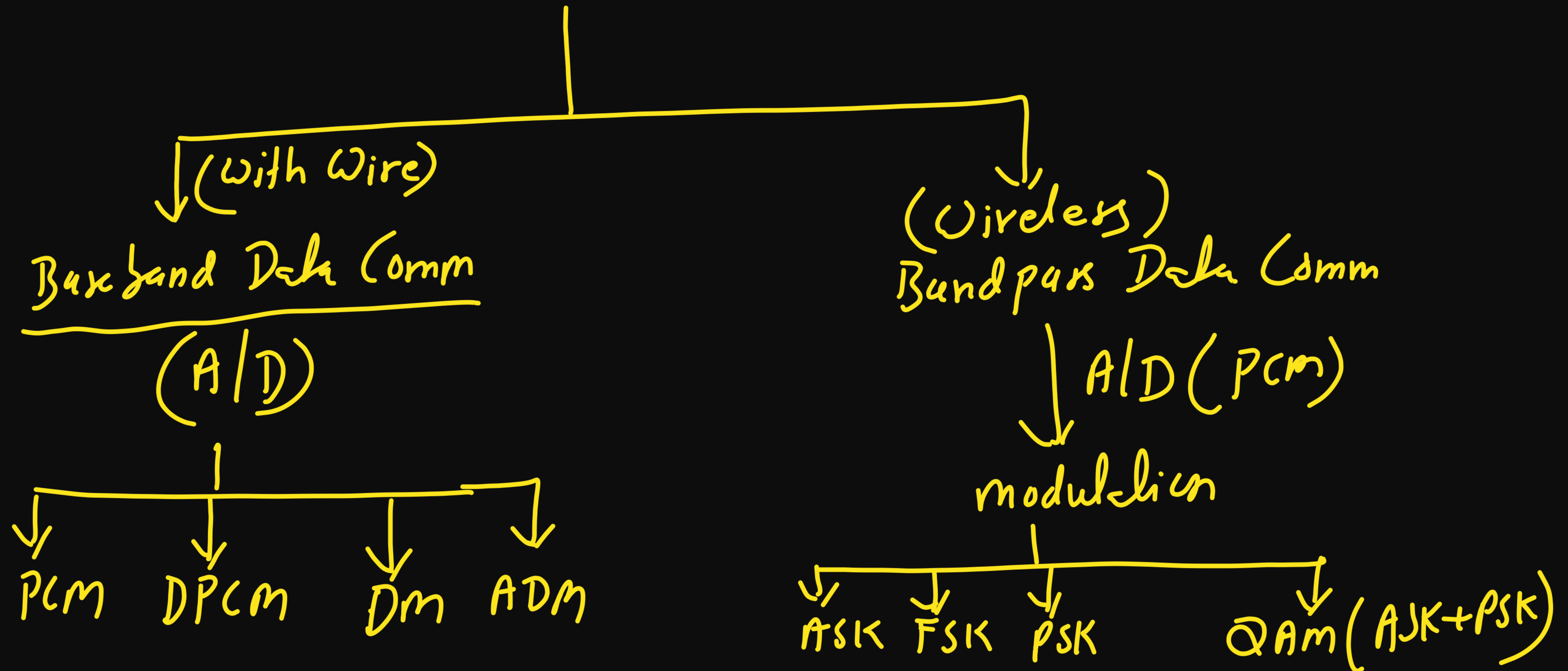


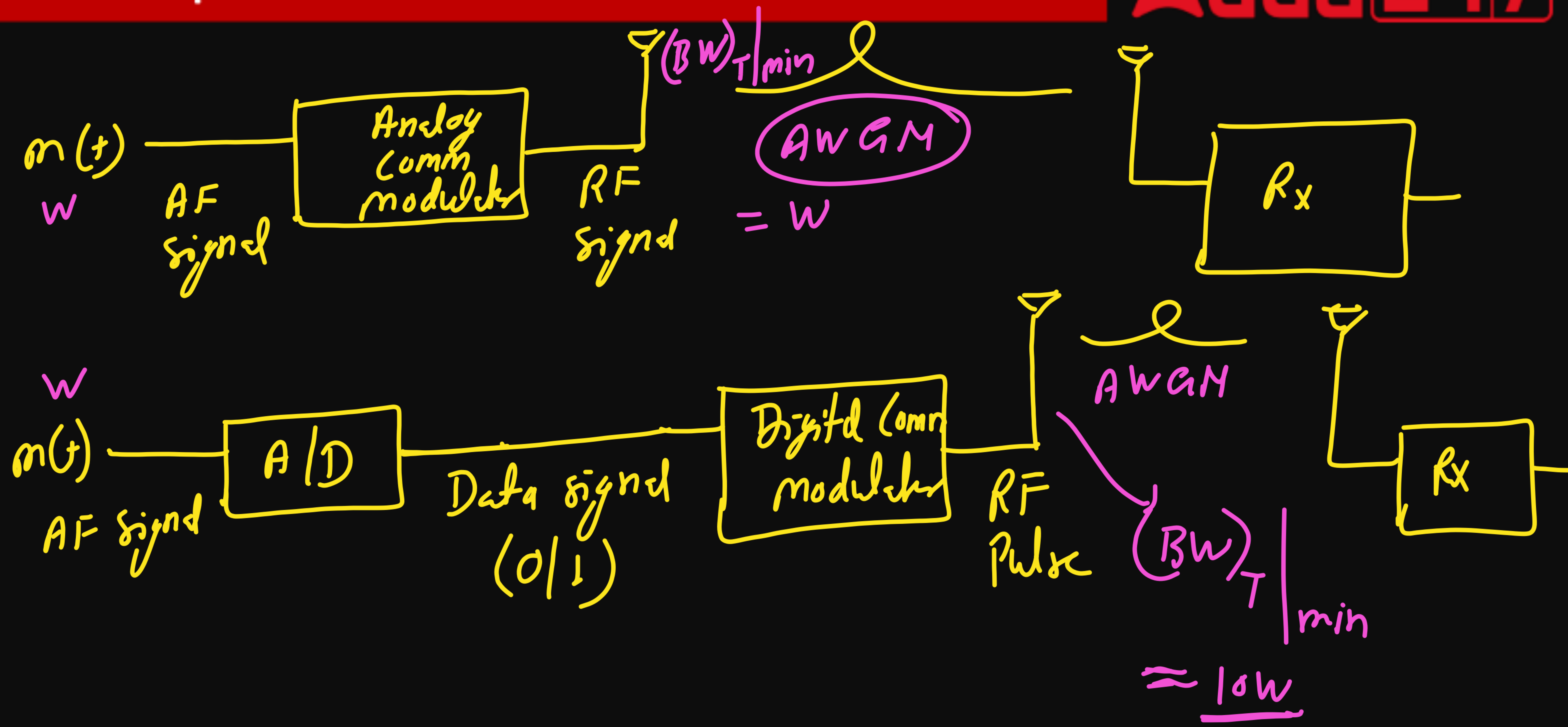
NETWORK THEORY	SATURDAY Live @11AM	RAVI SIR
COMMUNICATION	WEDNESDAY Live @8PM	RENU SIR
ANALOG ELECTRONICS	THURSDAY Live @8PM	LAWRENCE SIR
ENGINEERING MATHEMATICS	FRIDAY Live @11AM	ANANT SIR
ELECTRICAL MACHINE	MONDAY Live @8PM	SANTAN SIR

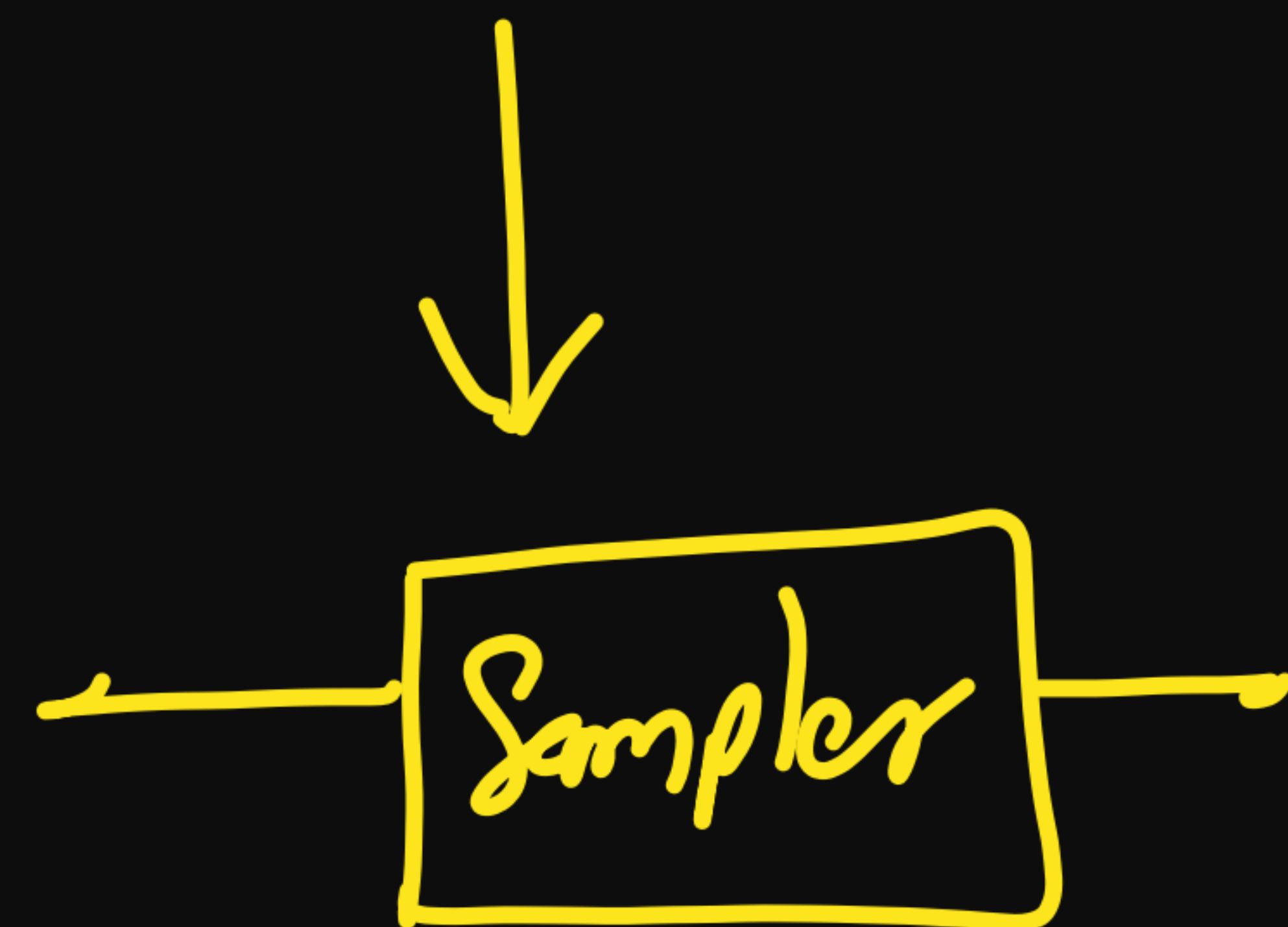
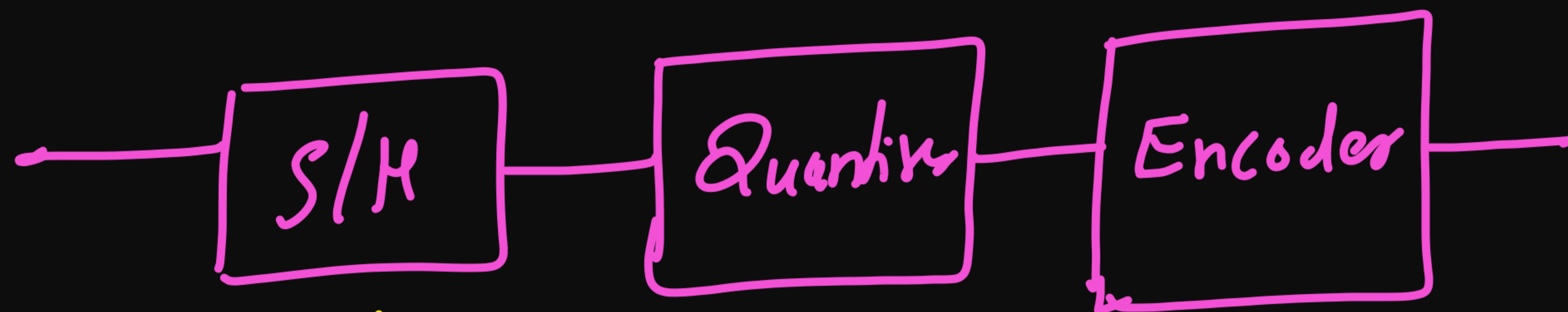




Digital Comm







- (i) Sampling Theorem
 - (ii) Quantiser
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} Imp. }


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